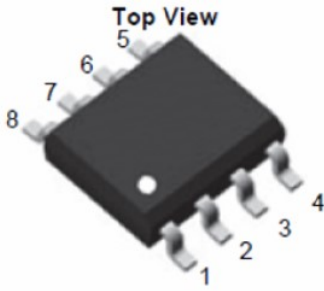
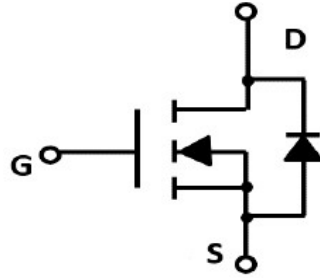
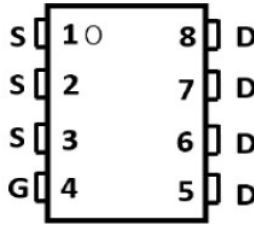


N-Channel Enhancement Mode Field Effect Transistor



SOP-8



Product Summary

- V_{DS} 20V
- I_D 10A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 13.5mohm
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) < 17mohm
- $R_{DS(ON)}$ (at $V_{GS}=1.8V$) < 25mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High Power and current handling capability
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	20	V
Gate-source Voltage	V_{GS}	± 10	V
Drain Current	I_D	$T_A=25^\circ C$	10
		$T_A=70^\circ C$	8
Pulsed Drain Current ^A	I_{DM}	45	A
Total Power Dissipation	P_D	$T_A=25^\circ C$	1.9
		$T_A=70^\circ C$	1.2
Thermal Resistance Junction-to-Ambient ^B	$R_{\theta JA}$	66	$^\circ C/W$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS10N02A	F2	Q10N02	4000	8000	64000	13" reel



YJS10N02A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.45	0.62	1.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =10A		11	13.5	mΩ
		V _{GS} =2.5V, I _D =4A		14	17	
		V _{GS} =1.8V, I _D =2A		18.2	25	
Diode Forward Voltage	V _{SD}	I _S =10A, V _{GS} =0V			1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, f=1MHZ		888		pF
Output Capacitance	C _{oss}			133		
Reverse Transfer Capacitance	C _{rss}			117		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =4.5V, V _{DS} =10V, I _D =6.8A		11.05		nC
Gate-Source Charge	Q _{gs}			1.73		
Gate-Drain Charge	Q _{gd}			3.1		
Turn-on Delay Time	t _{D(on)}	V _{GS} =4.5V, V _{DS} =10V, I _D =6.8A R _{GEN} =3Ω		7		ns
Turn-on Rise Time	t _r			46		
Turn-off Delay Time	t _{D(off)}			30		
Turn-off fall Time	t _f			52		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics



Figure1. Output Characteristics

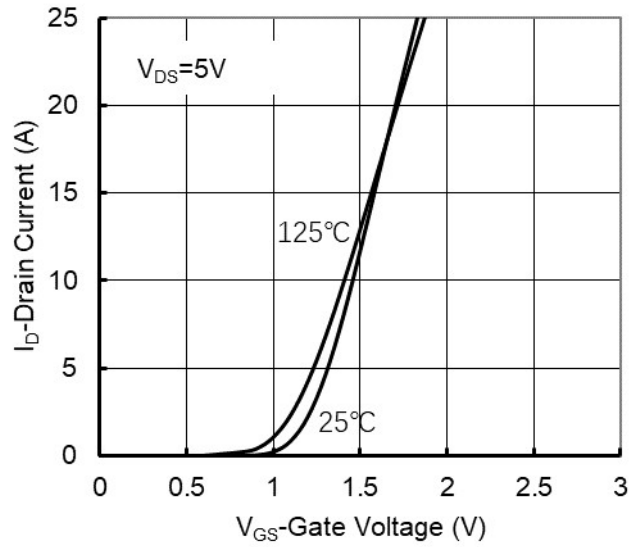


Figure2. Transfer Characteristics



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

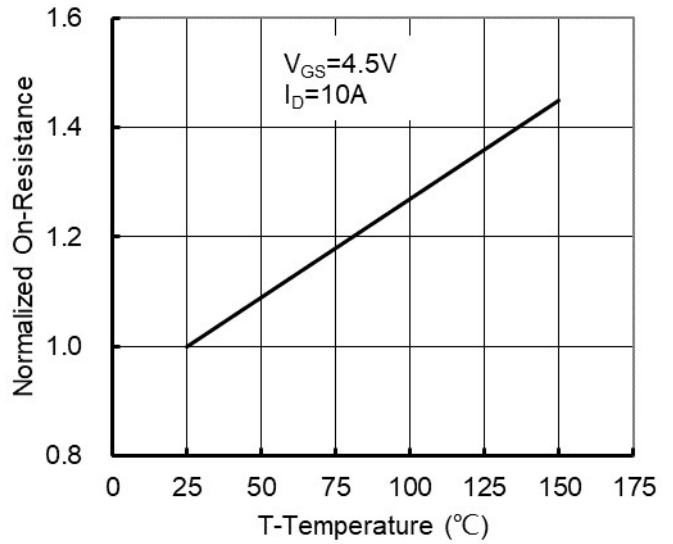


Figure 4: On-Resistance vs. Junction Temperature

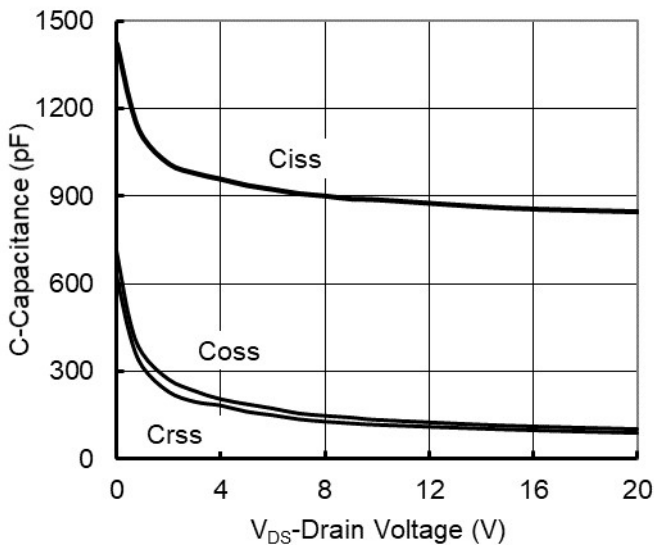


Figure5. Capacitance Characteristics

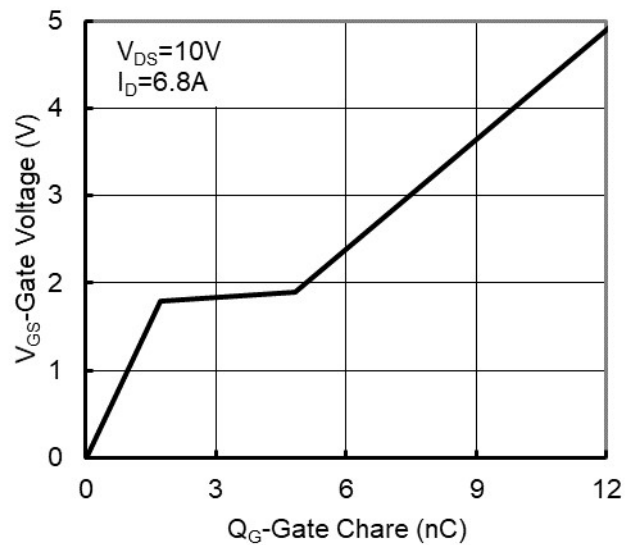


Figure6. Gate Charge



YJS10N02A

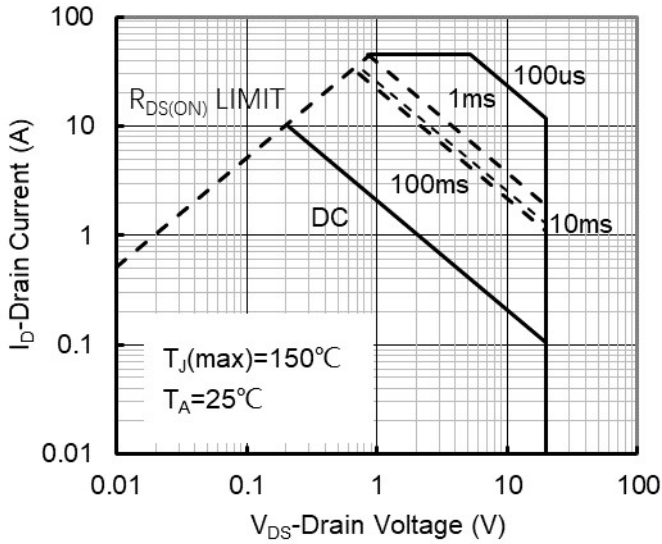


Figure7. Safe Operation Area

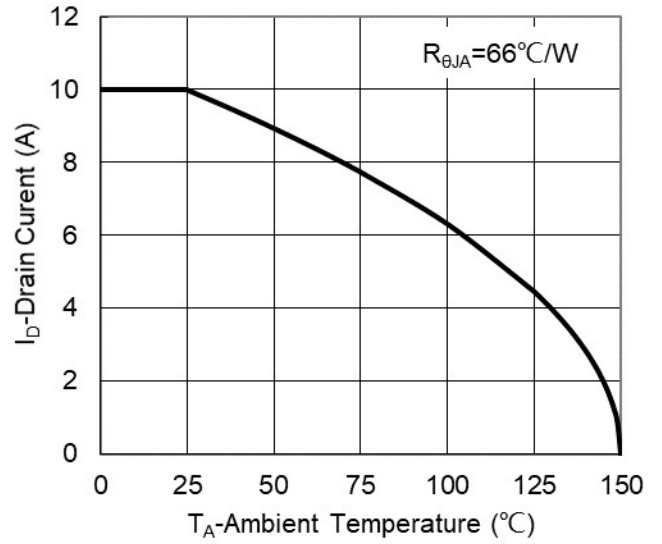


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

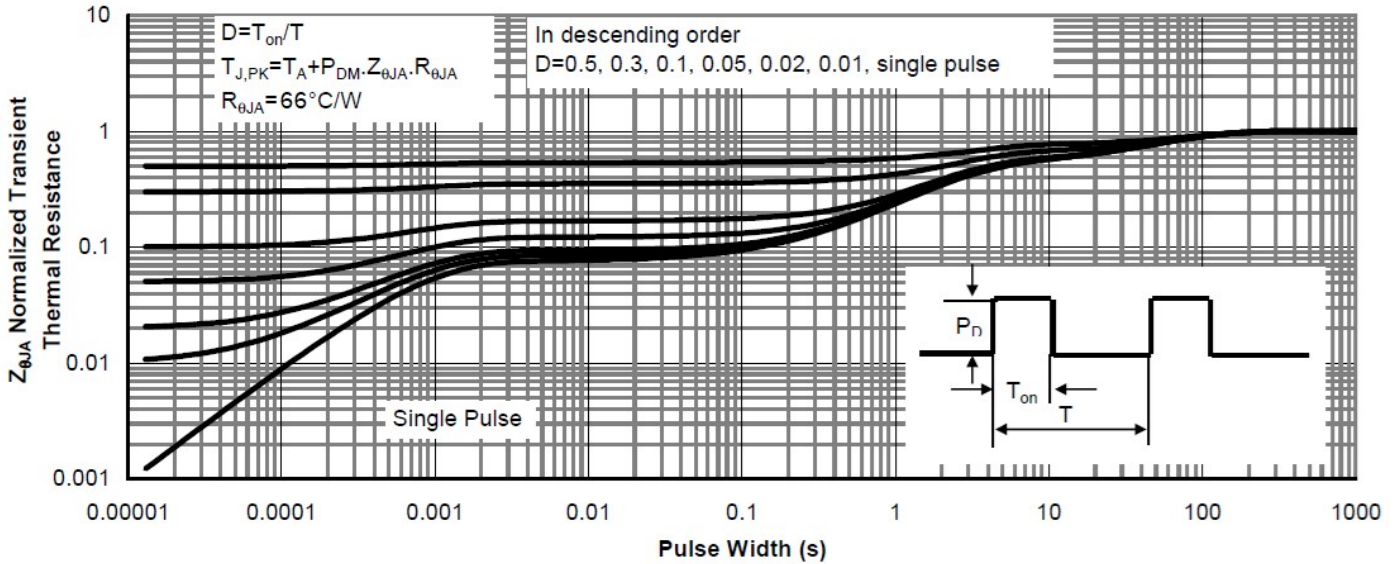


Figure9. Normalized Maximum Transient Thermal Impedance



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

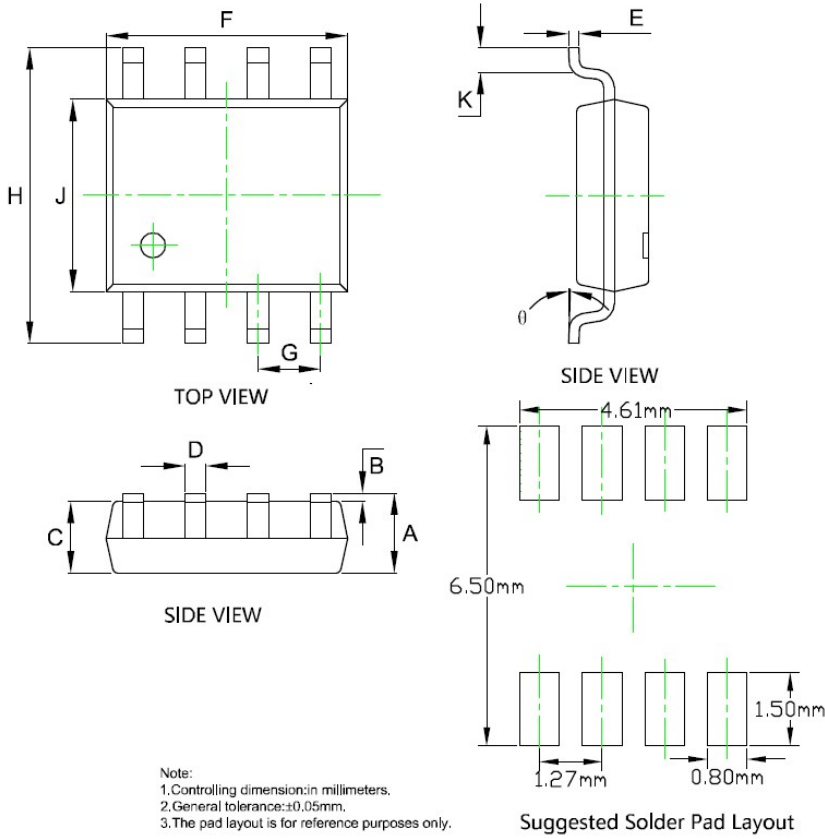


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



YJS10N02A

■ SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°



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